WHAT IS CLAIMED IS:

1. A probe card for testing a semiconductor wafer comprising:

a substrate comprising a contact member and a first conductor formed on the substrate in electrical communication with the contact member; and

a membrane for physically and electrically attaching the substrate to a test fixture, said membrane comprising tape with a second conductor thereon electrically attached to the first conductor.

2. The probe card as claimed in claim 1 and further comprising a compressible member mounted to a surface of the substrate.

3. The probe card as claimed in claim 1 and further comprising a leveling mechanism for leveling the substrate with respect to the wafer.

4. The probe card as claimed in claim 1 and further comprising a mounting plate for mounting the substrate to a testing apparatus.

5. The probe card as claimed in claim 1 and wherein the first conductor includes a bonding pad formed on a recessed portion of the substrate.

6. The probe card as claimed in claim 1 and wherein the substrate includes a plurality of contact members for contacting all of the dice on the wafer at a same time.

7. The probe card as claimed in claim 1 and wherein the contact member comprises an element selected from the group

consisting of a raised member etched from the substrate, an indentation formed in the substrate covered with a conductive layer, and a compliant pin attached to the substrate.

8. A probe card for testing a semiconductor wafer having a bumped contact location comprising:

a substrate comprising a contact member configured to electrically connect to the bumped contact location, said contact member comprising an indentation formed in the substrate and covered with a conductive layer; and

a membrane for mounting the substrate to a test fixture, said membrane comprising tape with a conductor thereon configured to establish electrical communication with the conductive layer.

9. The probe card as claimed in claim 8 and further comprising a compressible member mounted to a surface of the substrate.

10. The probe card as claimed in claim 8 and wherein the indentation comprises a depression sized to retain the bumped contact location.

11. The probe card as claimed in claim 8 and wherein the indentation includes a projection configured to penetrate into the bumped contact location.

12. A probe card for testing semiconductor dice contained on a wafer, comprising:

a substrate comprising a pattern of contact members configured to electrically contact a pattern of contact locations on the wafer, said contact members comprising raised members covered with conductive layers in electrical communication with a pattern of conductors;

a compressible member attached to a surface of the substrate; and

a membrane for attaching the substrate to a testing apparatus, said membrane comprising an elastomeric tape having a second pattern of conductors attached thereto, said second pattern of conductors in electrical communication with test circuitry and bonded to the pattern of conductors on the substrate.

13. The probe card as claimed in claim 12 and wherein the second pattern of conductors is bonded to the pattern of conductors on the substrate using a member selected from the group consisting of metal microbumps, conductive adhesives and bond wires.

14. The probe card as claimed in claim 12 and further comprising a mounting plate for mounting the substrate to the membrane.

15. The probe card as claimed in claim 12 and further comprising a leveling mechanism for leveling the substrate with respect to the wafer.

16. The probe card as claimed in claim 12 and further comprising a socket attached to the testing apparatus and wherein the substrate includes terminal contacts configured to insert into the socket.

17. A probe card for testing semiconductor dice contained on a wafer, comprising:

a mounting plate including a first conductor formed thereon;

a substrate attached to the mounting plate comprising a raised contact member covered with a conductive layer in electrical communication with a second conductor;

an electrical path formed between the first conductor and the second conductor; and

an electrically insulating tape having a third conductor formed thereon, said third conductor electrically connected to the first conductor.

18. The probe card as claimed in claim 17 and further comprising a compressible member attached to a surface of the substrate.

19. The probe card as claimed in claim 17 and wherein the electrical path comprises a wire bond.

20. A probe card for testing a semiconductor wafer comprising:

a substrate comprising a contact member configured to retain and electrically connect to a bumped contact location on the wafer, said contact member comprising a compliant pin attached to the substrate; and

a membrane for mounting the interconnect substrate to a test fixture, said membrane comprising polymer tape with a metal foil conductor attached thereto configured to establish electrical communication with the conductive layer.

21. The probe card as claimed in claim 20 and wherein the compliant pin comprises a spring segment.

22. A probe card for testing semiconductor dice contained on a wafer, comprising:

a substrate comprising a plurality of patterns of contact members configured to electrically connect to a plurality of patterns of contact locations on the dice;

said contact members comprising raised members with penetrating projections sized and shaped to penetrate the contact locations to a self limiting penetration depth;

said contact members further comprising conductive layers in electrical communication with a first pattern of conductors formed on the substrate;

a mounting plate attached to the substrate comprising a second pattern of conductors bonded to the first pattern of conductors; and

a membrane comprising an electrically insulating tape with a third pattern of conductors formed thereon bonded to the first pattern of conductors on the mounting plate.

23. The probe card as claimed in claim 21 and wherein the first pattern of conductors is bonded to the second pattern of conductors by wire bonding.

24. The probe card as claimed in claim 21 and wherein the mounting plate comprises a socket for receiving external contacts on the substrate in electrical communication with the contact members.

25. The probe card as claimed in claim 24 and wherein the external contacts comprise pads or balls arranged in a grid array.

26. The probe card as claimed in claim 25 and wherein the external contacts comprise pins arranged in a pin grid array.

27. A probe card for testing semiconductor dice contained on a semiconductor wafer comprising:

a substrate configured to test every die on the wafer at a same time, said substrate comprising a plurality of raised contact members covered with conductive layers, said substrate further comprising a plurality of conductors in electrical communication with the contact members, said contact members including projections sized and shaped to penetrate into contact locations on the wafer while surfaces of the contact members limit further penetration; and

a membrane for physically and electrically connecting the substrate to a testing apparatus, said membrane comprising an electrically insulating tape having a pattern of conductors formed thereon bonded to the plurality of conductors on the substrate.

28. The probe card as claimed in claim 27 and further comprising a compressible member attached to a surface of the substrate.

29. The probe card as claimed in claim 28 and wherein the compressible member comprises a material selected from the class consisting of silicone, butyl rubber, fluorosilicone and metal filled elastomers.

30. The probe card as claimed in claim 27 and wherein the conductive layers comprise a non-oxidizing material.

31. The probe card as claimed in claim 27 and wherein the penetrating projections have a height that is less than a thickness of the contact locations.

32. The probe card as claimed in claim 27 and further comprising a pressure plate in contact with the compressible member.

33. A probe card for testing semiconductor dice contained on a wafer, comprising:

a substrate comprising a plurality of patterns of contact members configured to electrically connect to a plurality of patterns of contact locations on the dice;

a plurality of external contacts formed on the substrate in electrical communication with the contact members;

a mounting plate for mounting the substrate to a testing apparatus, said mounting plate including a pattern of conductors configured to electrically contact the external contacts on the substrate; and

a membrane bonded to the mounting plate for providing electrical paths from test circuitry to the conductors on the mounting plate.

34. The probe card as claimed in claim 33 and wherein the external contacts comprise pads or balls formed in a grid array.

35. The probe card as claimed in claim 33 and wherein the mounting plate comprises an electrical socket.

36. The probe card as claimed in claim 33 and further comprising a compressible member attached to the substrate.

37. A probe card for testing semiconductor dice contained on a wafer, comprising:

a mounting plate having a sealed space formed therein;

a substrate comprising a plurality of patterns of contact members configured to electrically connect to a

plurality of patterns of contact locations on the dice, said substrate slidably mounted to the mounting plate within the sealed space;

a gas supply in flow communication with the sealed space for exerting a biasing force on the substrate; and

a membrane bonded to the mounting plate for providing electrical paths from test circuitry to the contact members.

38. The probe card as claimed in claim 37 and further comprising a leveling mechanism for leveling the substrate with respect to the wafer.

39. The probe card as claimed in claim 38 and wherein the leveling mechanism includes leveling screws or shims.

40. The probe card as claimed in claim 38 and wherein the leveling mechanism includes leveling springs.

41. A probe card for testing a semiconductor wafer comprising:

a substrate comprising a plurality of contact members in electrical communication with a first pattern of conductors;

a membrane for physically and electrically attaching the substrate to a test fixture, said membrane comprising tape with a second pattern of conductors thereon bonded to the first pattern of conductors; and

a leveling mechanism for planarizing the contact members with respect to the wafer.

42. The probe card fixture as claimed in claim 41 and wherein the leveling mechanism comprises screws and a leveling plate in contact with the substrate.

43. The probe card fixture as claimed in claim 41 and further comprising a compressible member attached to the substrate.

44. A method for testing a semiconductor wafer comprising:

providing a testing apparatus comprising a force applying mechanism and test circuitry;

providing a substrate comprising contact members configured to establish temporary electrical communication with contact locations on the wafer, said contact members comprising raised members with penetrating projections;

bonding a membrane to the substrate and testing apparatus, said membrane configured to provide an electrical path to the contact members and to mount the substrate to the testing apparatus;

biasing the substrate against the wafer; and

applying test signals through the membrane and contact members to the contact locations on the wafer.

45. The method as claimed in claim 44 and wherein the substrate includes contact members for contacting each die on the wafer at a same time and the test signals are electronically switched to selected dice.

46. The method as claimed in claim 44 and further comprising mounting a compressible member between the force applying mechanism and substrate.

47. The method as claimed in claim 44 and wherein the membrane comprises electrically insulating tape having conductors and microbumps for bonding to the substrate.

48. A method for testing a semiconductor wafer comprising:

providing a testing apparatus comprising a force applying mechanism and test circuitry;

providing a substrate comprising indentation contact members configured to retain bumped contact locations on the wafer and to establish temporary electrical communication with the bumped contact locations;

bonding a membrane to the substrate and testing apparatus, said membrane configured to provide an electrical path to the contact members and to mount the substrate to the testing apparatus;

biasing the substrate against the wafer; and

applying test signals through the membrane and contact members to the contact locations on the wafer.

49. The method as claimed in claim 48 and further comprising mounting a compressible member to a backside of the substrate for cushioning a pressure applied to the substrate by the force applying mechanism.

50. The method as claimed in claim 48 and wherein the substrate comprises silicon.

51. A method for testing semiconductor dice comprising:

providing a probe card comprising a substrate with a raised contact member covered with a conductive layer in electrical communication with a conductor, said raised contact member having a height of from 10μm to 100μm, and having a penetrating projection formed thereon with a height of from .1μm to 1μm, said projection configured to penetrate a contact location on the wafer to a limited penetration depth;

physically and electrically connecting the probe card to a testing apparatus using a membrane having a second conductor bonded to the conductor on the substrate; and

applying test signals through the second conductor, through the conductor, and through the contact member to the contact locations.

52. The method as claimed in claim 51 and further comprising mounting a compressible member between the force applying mechanism and substrate.

53. The method as claimed in claim 51 and further comprising applying pressure from the testing apparatus through a pressure plate in contact with the compressible member.

54. The method as claimed in claim 51 and wherein the second conductor is bonded to the conductor by heating a metal microbump therebetween.

55. The method as claimed in claim 51 and wherein the second conductor is bonded to the conductor by applying a conductive adhesive therebetween.

56. A method for testing a semiconductor wafer having a plurality of semiconductor dice, said method comprising:

providing a testing apparatus configured to apply test signals to the dice;

providing a substrate including a plurality of contact members configured to electrically connect to all of the dice on the wafer at a same time; and

providing a membrane for mounting and electrically connecting the substrate to the test fixture, said membrane comprising electrically insulating tape with a plurality of

conductors thereon configured to establish electrical communication with the contact members;

applying test signals through the contact members to at least one selected die on the wafer; and

electronically switching the test signals to another die on the wafer.

57. A system for testing a semiconductor wafer, comprising:

a testing apparatus comprising test circuitry and a force applying mechanism;

a substrate comprising a raised contact member having a penetrating projection configured to penetrate a contact location on the wafer and a surface configured to limit a penetration depth of the penetration projection into the contact location; and

a membrane for mounting and electrically connecting the substrate to the test fixture, said membrane comprising electrically insulating tape with a conductor thereon configured to establish electrical communication with the contact member.

58. The system as claimed in claim 57 and further comprising a compressible member mounted to a backside of the substrate for cushioning a pressure applied to the substrate by the force applying mechanism.

59. The system as claimed in claim 57 and wherein the substrate comprises a plurality of contact members for contacting from one die to all dice on the wafer at a same time.

60. The system as claimed in claim 57 and wherein the substrate comprises a plurality of contact members for

contacting all dice at a same time, and test signals are electronically applied to selected dice.

61. A system for testing a semiconductor wafer;

a testing apparatus comprising test circuitry, a probe card fixture and a force applying mechanism;

a substrate mounted to the probe card fixture, said substrate comprising a raised contact member covered with a conductive layer in electrical communication with a conductor, said raised contact member having a height of from 10μm to 100μm, and having a penetrating projection formed thereon with a height of from .1μm to 1μm, said projection configured to penetrate a contact location on the wafer to a limited penetration depth; and

a membrane for physically and electrically connecting the substrate to the probe card fixture, said membrane comprising polyimide having a copper conductor formed thereon bonded to the conductor on the substrate.

62. The system as claimed in claim 61 and wherein the copper conductor is bonded to the conductor by bonding a metal microbump therebetween.

63. The system as claimed in claim 61 and wherein the copper conductor is bonded to the conductor by applying a conductive adhesive therebetween.

64. The system as claimed in claim 61 and further comprising a compressible member mounted to a backside of the substrate.

65. The system as claimed in claim 61 and further comprising a pressure plate in contact with the member and with the force applying mechanism.

66. The system as claimed in claim 61 and wherein the conductor includes a bonding pad for bonding to the copper conductor, said bonding pad formed adjacent to a stepped edge of the substrate.

67. The system as claimed in claim 61 and wherein the conductive layer comprises a material that in non-reactive with a material of the contact location.

68. A system for testing a semiconductor wafer, containing semiconductor dice, comprising:

a testing apparatus comprising test circuitry and a force applying mechanism;

a substrate comprising a contact member configured to retain and electrically connect to a bumped contact location on the wafer, said contact member comprising an indentation covered with a conductive layer;

a membrane for mounting and electrically connecting the substrate to the test fixture, said membrane comprising electrically insulating tape with a conductor thereon configured to establish electrical communication with the contact member.

69. The system as claimed in claim 68 and wherein the indentation comprises a concave depression sized to retain the bumped contact location.

70. The system as claimed in claim 68 and wherein the indentation has an inside diameter of from 1 mils to 10 mils.

71. The system as claimed in claim 68 and wherein the conductive layer is formed of a non-oxidizing material.

72. A system for testing a semiconductor wafer, comprising:

a testing apparatus comprising test circuitry and a force applying mechanism;

a substrate including a contact member comprising a compliant member configured to electrically connect to a contact location on the wafer; and

a membrane for mounting and electrically connecting the substrate to the test fixture, said membrane comprising a polymer film with a metal foil conductor thereon configured to establish electrical communication with the contact member.

73. The system as claimed in claim 72 and wherein the contact member comprises a pin attached to the substrate and shaped as a spring segment.